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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,278	WU ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-78* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,15-42,44-63 and 65-76* is/are rejected.

7)☒ Claim(s) *10-14,43,64,77 and 78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/14/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-2, 3A and 3B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 35, 46-47 and 49 are rejected under 35 U.S.C. 102(b) as being anticipated by Hill U.S. 6,031,428.

Regarding claim 1, Hill invention is directed to a Steered Frequency Phase Lock Loop (SFPLL) comprising a phase loop that functions like a normal phase locked loop (PLL) and locks to the input signal, and a frequency loop that uses a reference

frequency to influence the phase loop and effectively confines the output frequency of the phase loop and the SFPLL to be in a range of frequencies close to the reference frequency.

In column 3 lines 15-30, FIG. 1 shows a SFPLL including a clock phase adjustment circuit comprising a phase detector 10, a first gain component 12, a first filter component 14; a clock frequency adjustment circuit including a frequency detector 22, a second gain component 24 and a third filter component 26.

Regarding claim 35, claim is rejected on the same ground as for claim 1 because of similar scope.

Regarding claim 46, claim is rejected on the same ground as for claim 1 because of similar scope.

Regarding claim 47, in FIG. 1, Hill discloses the SFPLL includes a phase detector 10 and a frequency detector 22 for sampling the data streams at a predetermined times.

Regarding claim 49, in FIG. 1, Hill discloses the SFPLL includes a phase detector 10 and a frequency detector 22 for providing phase information and frequency information.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-9, 36-42 and 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hill U.S. 6,031,428 in view of Doblar U.S. Patent 6,731,709 B2.

Regarding claim 2, as recited in claim 1 above, the clock frequency adjustment circuit includes frequency detector 22, a second gain component 24 and third filter component 26. As common knowledge of one of ordinary skill in the art, the second gain component 24 includes the frequency detector gain K_{fd} and a multiplier.

Hill, however, does not disclose an integrator as claimed in the application claim.

Doblar teaches a similar phase locked loop (PLL) as shown in FIG. 3 wherein a loop filter 316 is coupled to receive the phase error signal and to output an error correction signal to a voltage controller oscillator (VCO) 318. In a preferred embodiment, Doblar teaches that the loop filter comprises an active low-pass filter configured as an integrator. As common knowledge of one of ordinary skill in the art, because the low-pass filter and integrator can be used interchangeably, therefore, one of ordinary skill in the art at the time the invention was made would have recognized the third filter component 26 in Hill teachings can be implemented as an integrator.

Regarding claim 3, referring to FIG. 1, as recited in claim 2, the second gain component 24 includes the frequency detector gain K_{fd} and a multiplier, wherein the multiplier receives the clock frequency information from frequency detector 22 as shown in FIG. 1.

Regarding claim 4, the second gain component 24 and third filter component 26 are in series.

Regarding claim 5, third filter component 26 provides clock frequency adjustment signal as claimed.

Regarding claim 6, FIG. 7 is a functional block schematic circuit diagram of a phase detector for an application of the SFPLL to timing recovery from a NRZ data stream.

Regarding claim 7, Hill does not explicitly disclose the clock frequency information comprising an undershoot determination and an overshoot determination as set forth in the application claim.

Nevertheless, as disclosed in column 1 lines 25-50, Hill further teaches that the Steered Frequency Phase Lock Loop (SFPLL) are that the output frequency is equal or close to the reference frequency when no input signal is present, and the range of frequencies to which the SFPLL can lock is confined to a region around the reference

frequency, and the phase and frequency instabilities of the VCO can be reduced. In order to keep the frequency within the range of frequencies to which the SFPLL can lock is confined to a region around the reference frequency, one of ordinary skill in the art at the time the invention was made that would have recognized that the frequency detector would determine any undershoot or overshoot and use the feedback loop as shown in FIG. 1 to keep the frequency within the range of frequencies to which the SFPLL can lock.

Regarding claim 8, using similar arguments as recited in claim 7, the phase detector 10 would detect and provide phase information indicative of either early or late clock phase determination use the feedback loop as shown in FIG. 1 to keep the phase within a desired phase range.

Regarding claim 9, Hill does not show logic configured as set forth in the application claim.

Referring back to FIG. 1, in column 3 lines 5-25, Hill discloses that the SFPLL receives as inputs the clock phase information Θ'_i and clock frequency information ω'_i. Furthermore, because Hill suggests that the SFPLL has applications in many diverse areas of electronics such as timing recovery in base-band digital transmission, one of ordinary skill in the art at the time the invention was made would have recognized that the input signal can be sampled (or digitized) at Nyquist rate and

provide the clock phase information Θ'_i and clock frequency information ω'_i to the SFPLL.

Regarding claim 36, claim is rejected on the same ground as for claim 2 because similar scope.

Regarding claim 37, claim is rejected on the same ground as for claim 6 because similar scope.

Regarding claim 38, claim is rejected on the same ground as for claim 7 because similar scope.

Regarding claim 39, claim is rejected on the same ground as for claim 8 because similar scope.

Regarding claims 40-41, claims are rejected on the same ground as for claim 9 because similar scope.

Regarding claim 42, in FIG. 1, Hill discloses a phase detector 10 for providing clock phase information.

Regarding claim 44, in FIG. 2, Hill discloses a clock phase recovery circuit includes adders 28 and 16.

Regarding claim 45, in FIG. 2, Hill discloses adders 28 and 16 configured to add outputs of means for adjusting clock phase and means for adjusting clock frequency.

4. Claims 15-20, 48, 50, 52, 60-63 and 65-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Filip U.S. Patent 6,081,572.

Regarding claim 15, in column 4 lines 40-65, FIG. 2 illustrates a PLL system 200 including a PLL 202 and a phase and frequency detector 204.

The PLL 202 includes a phase detector 206, a summer 208, a filter 210, and a VCO 212. The phase detector 206 and the phase and frequency detector 204 each receives input data at the respective input port IN1. Preferably, the input data is in NRZ data format. In addition, the phase detector 206 and the phase and frequency detector 204 each receives a VCO signal at respective input port IN2 from the VCO 212.

Filip does not show explicitly a clock phase adjustment circuit and a clock frequency adjustment circuit as set forth in claim 1.

However, because the phase detector 206 and the phase and frequency detector 204 each receives a VCO signal at respective input port IN2 from the VCO 212, one of ordinary skill in the art at the time the invention was made would have recognized that the phase detector 206 and the phase and frequency detector 204, each receives input data at the respective input port IN1 and a VCO signal at respective input port IN2 from the VCO 212, constitute the claimed clock phase adjustment circuit and a clock frequency adjustment circuit.

The summer 208 performs superposition operation of the two received signals and generates an output signal representing the sum of the two signals; see column 5 lines 1-15.

In column 4 lines 50-67, the phase detector 206, sampling the VCO signal with reference to the input data signal, and the phase and frequency detector 204, generating a frequency difference from the frequency difference dependent DC-offset signal at an output port FD and a lock signal at an output port LOCK, constitute the claimed clock recovery circuit.

Regarding claim 16, FIG. 3 illustrates the phase and frequency detector 204 in accordance with one embodiment of the present invention. The phase and frequency detector 204 includes a phase shifter 302, a pair of phase detectors 304 and 306, and a frequency detector 308, in which phase detectors 304 and 306, and a frequency detector 308 are implemented as flip-flops (latches) to sampled data at predetermined times, e.g. input data to CLKs of flip-flops 304 and 306 in FIG. 3.

Regarding claims 17-18, as recited in claim 16, because phase detectors 304 and 306 latch the data according the input data clock, see FIG. 3, at regular intervals corresponding to an integer fraction of the recovered clock signal.

Regarding claim 19, FIG. 4A shows details diagram of phase detectors in the phase and frequency detector. In FIG. 4A, the phase and frequency detector includes a plurality of logic gates.

Regarding claim 20, FIG. 2 includes PLL 202.

Regarding claim 48, claim is rejected on the same ground as for claim 16 because of similar scope.

Regarding claim 50, claim is rejected on the same ground as for claim 20 because of similar scope.

Regarding claim 52, claim is rejected on the same ground as for claim 20 because of similar scope.

Regarding claim 60, claim is rejected on the same ground as for claim 15 because of similar scope.

Regarding claim 61, claim is rejected on the same ground as for claim 16 because of similar scope.

Regarding claims 62-63, depending how accuracy one desires, a person of ordinary skill in the art would have recognized the sampling interval is a design selection.

Regarding claims 65-67, using analogous argument as in claims 62-63, a person of ordinary skill in the art would have recognized how often to sample is a design selection.

Regarding claim 68, referring to FIG. 2, using a feedback loop from output of VCO 212, the LOCK indicates when the phase is locked.

Regarding claim 69, after the LOCK indication, the phase is locked and provided to PD 206 receiving data stream.

Regarding claim 70, referring to FIG. 2, FD 204 adjusts the clock frequency information.

Regarding claims 71-72, FIG. 2 discloses both frequency and phase are altered by PD 206 and FD 204 via feedback loop.

Regarding claim 73, claim is rejected on the same ground as for claim 15 because of similar scope.

Regarding claim 74, FIG. 2 provides the clock signal.

Regarding claim 75, in FIG. 2, PD 206 provides data stream.

Regarding claim 76, claim is rejected on the same ground as for claim 68 because of similar scope.

5. Claims 21-34, 51 and 53-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over FIG. 1 admitted prior art in the original disclosure in view of Hill U.S. Patent 6,031,428.

Regarding claim 21, in paragraphs [0002] - [0003] of the original disclosure, FIG. 1 admitted prior art discloses a transceiver 10 including a transmitter 20 for transmitting a serial data stream from a coupled storage device to a network, and a receiver 30 for receiving a serial data stream from the network for subsequent processing, and a digital timing loop 40.

FIG. 1 admitted prior art does not teach the clock data recovery circuit of claim 1.

Hill teaches the clock data recovery circuit as recited in the rejection of claim 1. Because Hill suggests the SFPLL has applications in timing recovery in base-band digital transmission, therefore, one of ordinary skill in the art at the time the invention was made would have been motivated to modify transceiver 10 of admitted prior art to implement the SFPLL in the digital timing loop 40.

Regarding claim 22, FIG. 1 admitted prior art shows the transceiver 10 can be embodied on a single integrated circuit.

Regarding claim 23, FIG. 2 admitted prior art includes a PLL for generating a reference clock signal to the transmitter 20 and receiver 30.

Regarding claim 24, FIG. 2 admitted prior art further includes a function generator 112.

Regarding claim 25, FIG. 2 admitted prior art does not teach the function generator comprises a spread spectrum wave generator as claimed in the application claim.

Referring to FIG. 2, the function generator 112 for generating a function waveform. For spread spectrum applications, one of one of ordinary skill in the art at the time the invention was made would have been motivated to modify the function generator to include a spread spectrum wave generator as claimed in the application claim.

Regarding claim 26, FIG. 1 admitted prior art further includes a configuration block as claimed.

Regarding claim 27, claim is rejected on the same ground as for claim 21 because of similar scope. Furthermore, in paragraphs [0002] and [0003], the transceiver 10 includes a transmitter 20 and a receiver 30.

Regarding claim 28, in paragraph [0003], transmitter 20 and receiver 30 transmit/ receive a serial data stream.

Regarding claims 29-30 and 32, in paragraph [0003], admitted prior art further discloses subsequent processing for conversion to a parallel data stream and storage in the coupled storage device.

Regarding claim 31, in paragraph [0003], admitted prior art discloses that transmitter 20 transmit a serial data stream generated from coupled storage device to a network.

Regarding claim 33, claim is rejected on the same ground as for claim 27 because of similar scope.

Regarding claim 34, in paragraph [0003], admitted prior art discloses that transmitter 20 transmit a serial data stream generated from coupled storage device to a network.

Regarding claim 51, claim is rejected on the same ground as for claim 27 because of similar scope.

Regarding claim 53, FIG. 1 admitted prior art can be implemented on a single integrated circuit.

Regarding claim 54, claim is rejected on the same ground as for claim 27 because of similar scope.

Regarding claim 55, claim is rejected on the same ground as for claim 29 because of similar scope.

Regarding claim 56, claim is rejected on the same ground as for claim 30 because of similar scope.

Regarding claim 57, claim is rejected on the same ground as for claim 31 because of similar scope.

Regarding claim 58, claim is rejected on the same ground as for claim 29 because of similar scope.

Regarding claim 59, claim is rejected on the same ground as for claim 33 because of similar scope.

Allowable Subject Matter

6. Claims 10-14, 43, 64 and 77-78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu et al. U.S. Patent 6,055,286 discloses "Oversampling Rotational Frequency Detector".

Pate et al. U.S. Patent 6,531,926 discloses "Dynamic Control Of Phase-Locled Loop".

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Cong Tran 10/27/2006

Primary Examiner KHANH TRAN